This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

OIPE JC99
JUN 0 2 2004
PATENT & TRADEMARK OFFICE

FIG.1

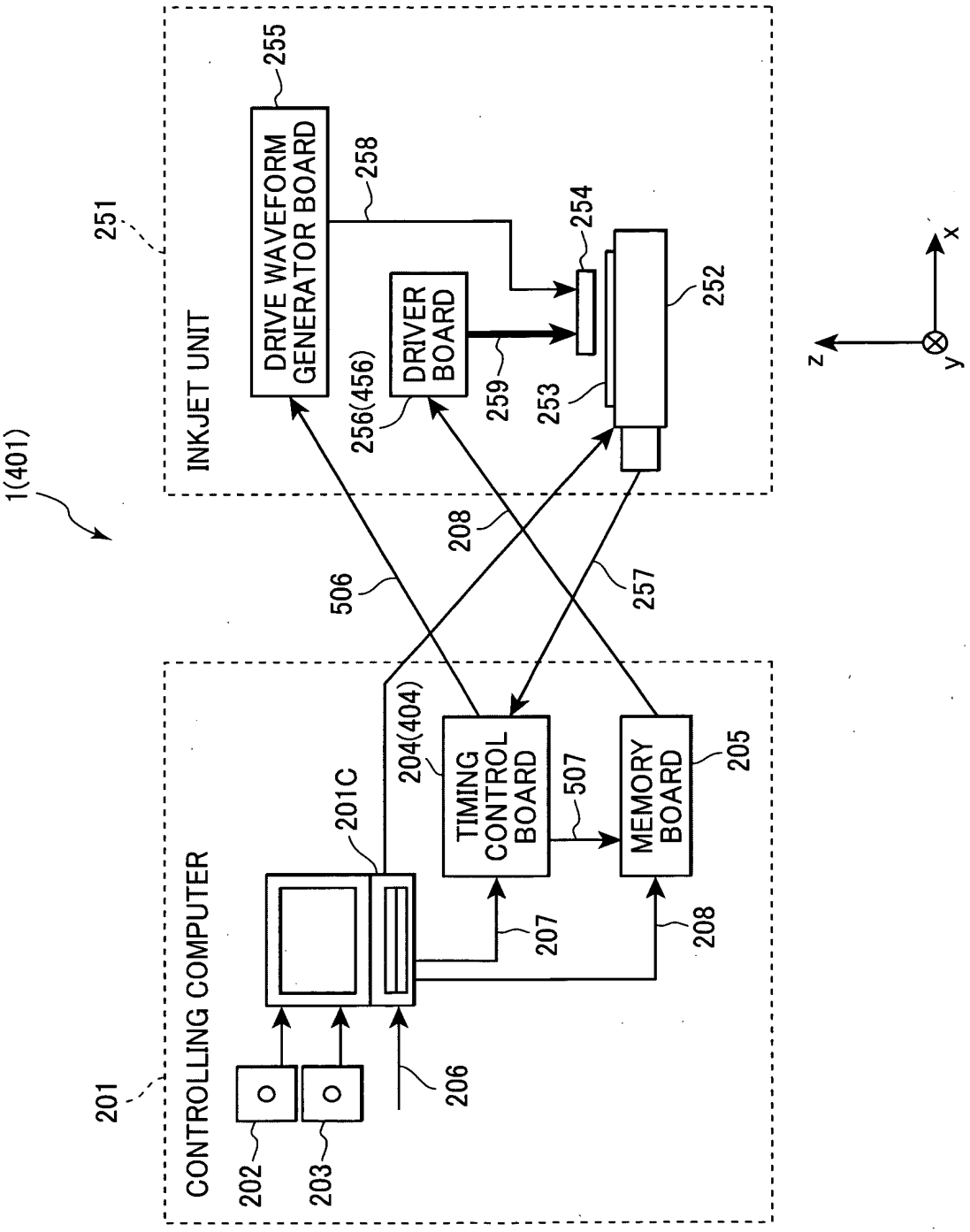


FIG.2

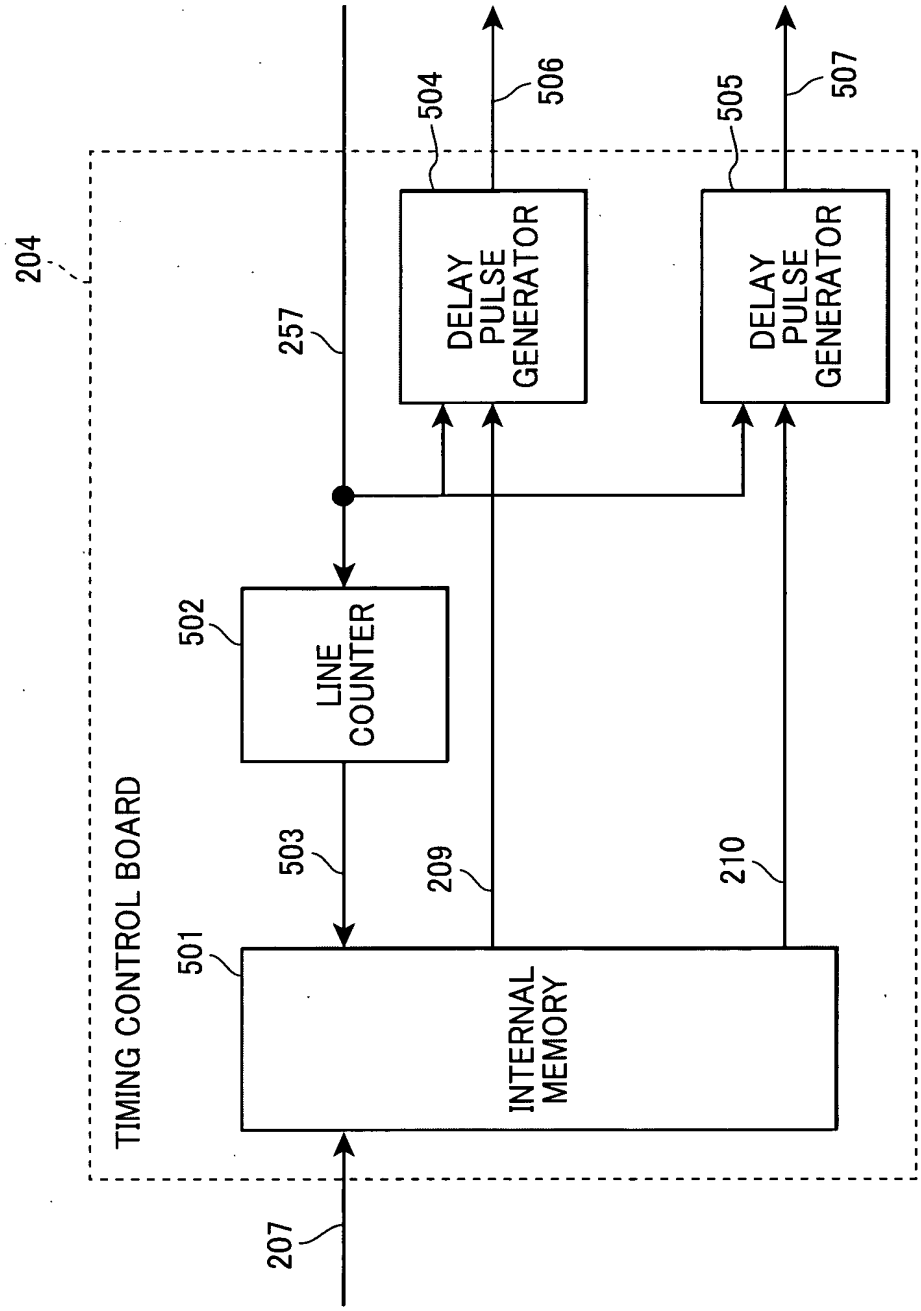

204
TIMING CONTROL BOARD
257
504
506
505
507
DELAY PULSE GENERATOR
DELAY PULSE GENERATOR
502
LINE COUNTER
503
209
210
501
INTERNAL MEMORY
207

FIG.3

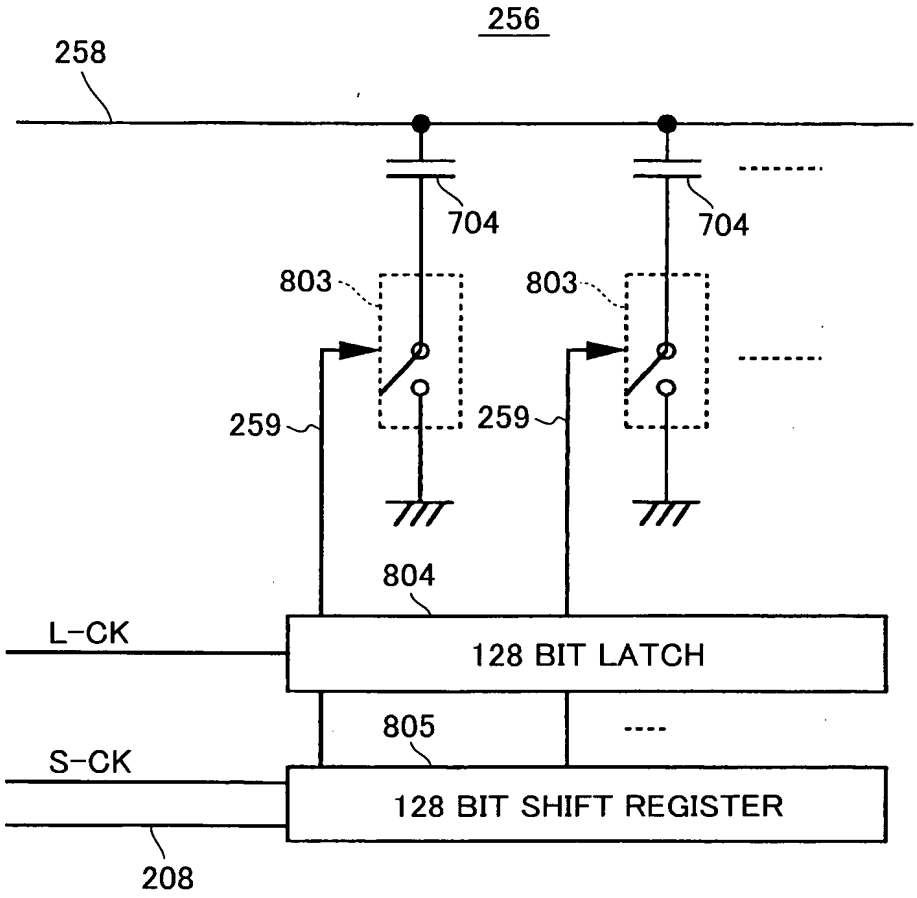

256
258
704
704
803
803
259
259
804
L-CK
128 BIT LATCH
805
S-CK
128 BIT SHIFT REGISTER
208

FIG.4

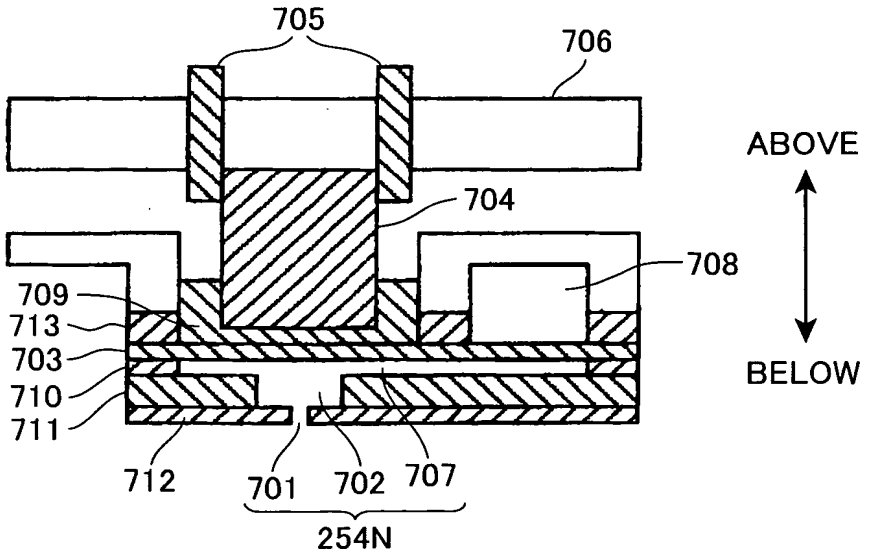

705
706
704
708
709
713
703
710
711
712
701
702
707
254N
ABOVE
BELOW

FIG.5(1)

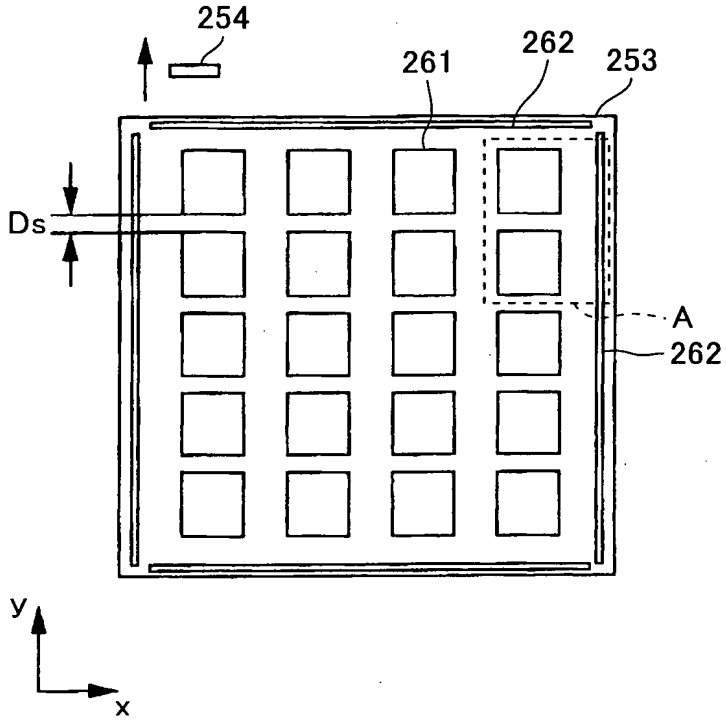

254
261
262
253
Ds
A
262
y
x

FIG.5(2)

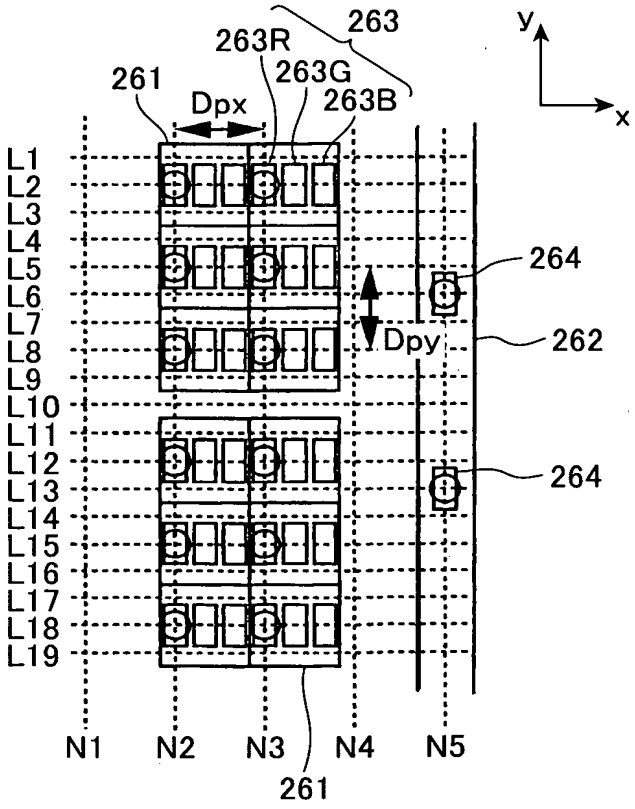

263
263R
263G
263B
261
Dpx
y
x
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
L13
L14
L15
L16
L17
L18
L19
264
Dpy
262
264
N1
N2
N3
N4
N5
261

FIG.6

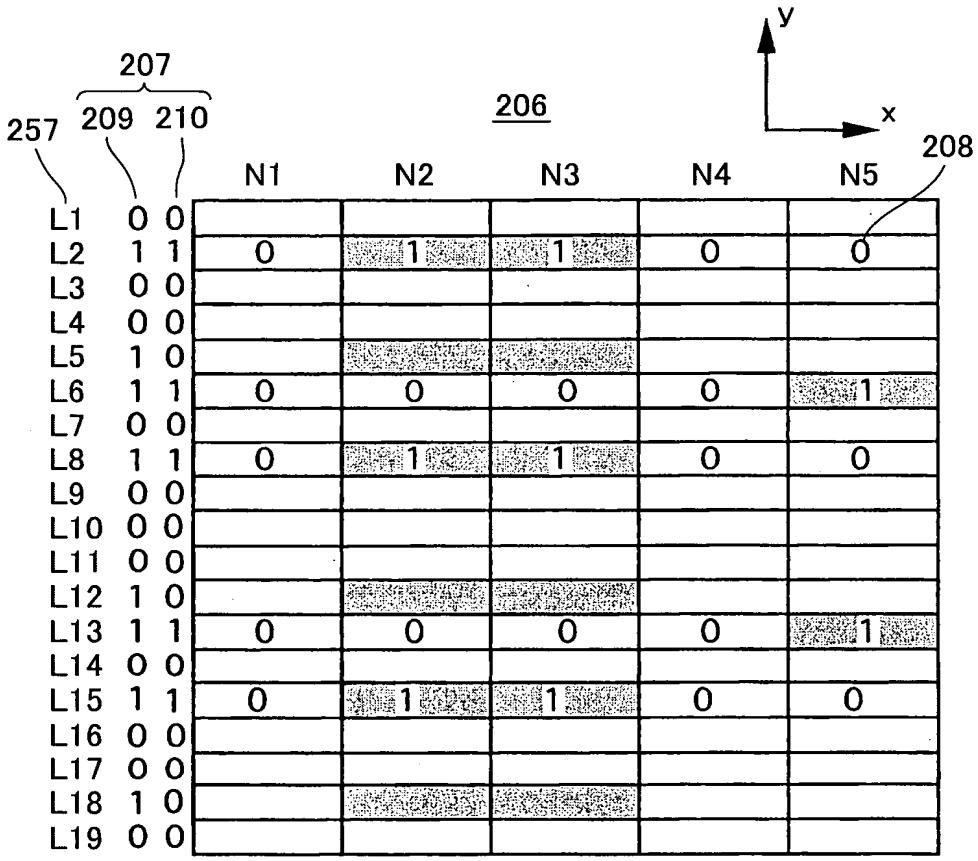

y
x
207
257
209
210
206
208
N1
N2
N3
N4
N5
L1 0 0
L2 1 1
L3 0 0
L4 0 0
L5 1 0
L6 1 1
L7 0 0
L8 1 1
L9 0 0
L10 0 0
L11 0 0
L12 1 0
L13 1 1
L14 0 0
L15 1 1
L16 0 0
L17 0 0
L18 1 0
L19 0 0
0 1 1 0 0
0 0 0 0 1
0 1 1 0 0
0 0 0 0 1
0 1 1 0 0

FIG.7(1)

207

0100 1101 0001 1010 010 ~ 209
0100 0101 0000 1010 000 ~ 210

208

(L2)01100
(L6)00001
(L8)01100
(L13)00001
(L15)01100

TOTAL OF 63 BIT

FIG.7(2)

(L1)00000
(L2)01100
(L3)00000
(L4)00000
(L5)01100
(L6)00001
(L7)00000
(L8)01100
(L9)00000
(L10)00000
(L11)00000
(L12)01100
(L13)00001
(L14)00000
(L15)01100
(L16)00000
(L17)00000
(L18)01100
(L19)00000

TOTAL OF 95 BIT

FIG.8

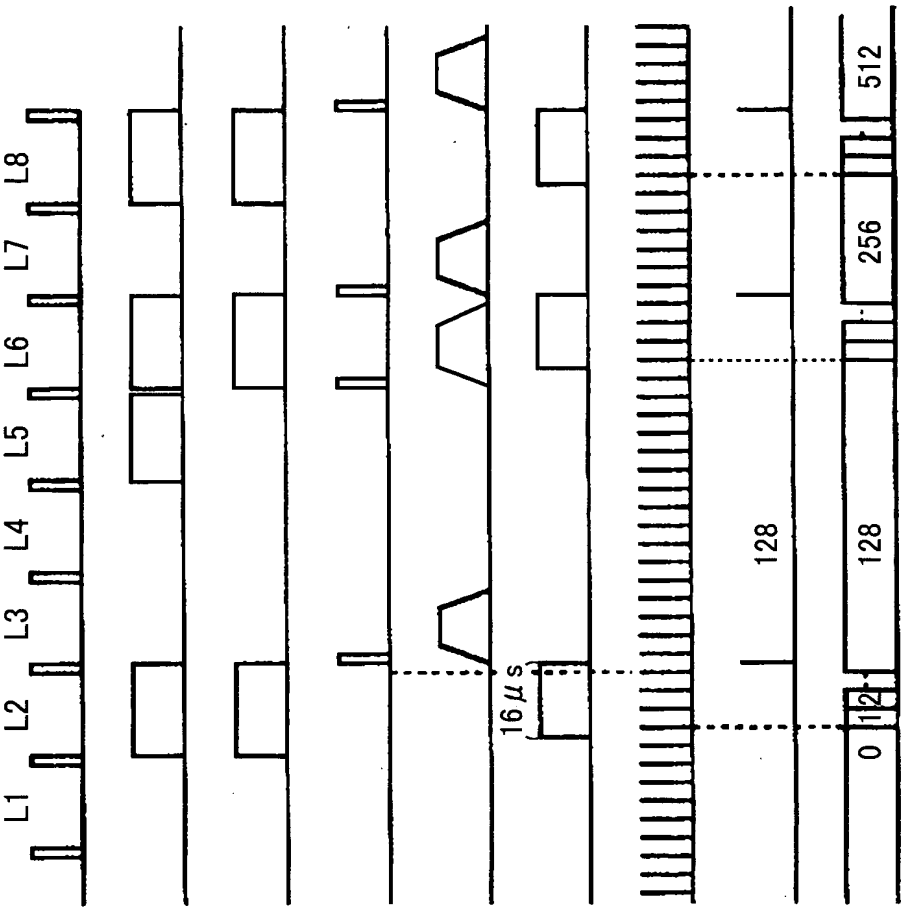

L1
L2
L3
L4
L5
L6
L7
L8
Y-DIRECTION ENCODER OUTPUT 257
DRIVE WAVEFORM GENERATION TIMING DATA 209
EJECTION DATA TRANSFER TIMING DATA 210
DRIVE WAVEFORM GENERATION TRIGGER SIGNAL 506
DRIVE WAVEFORM 258
16 μs
DATA TRANSFER REQUEST SIGNAL 507
SHIFT CLOCK S-CK
LATCH CLOCK-L-CK
128
EJECTION DATA 208
0
128
256
512

FIG.9

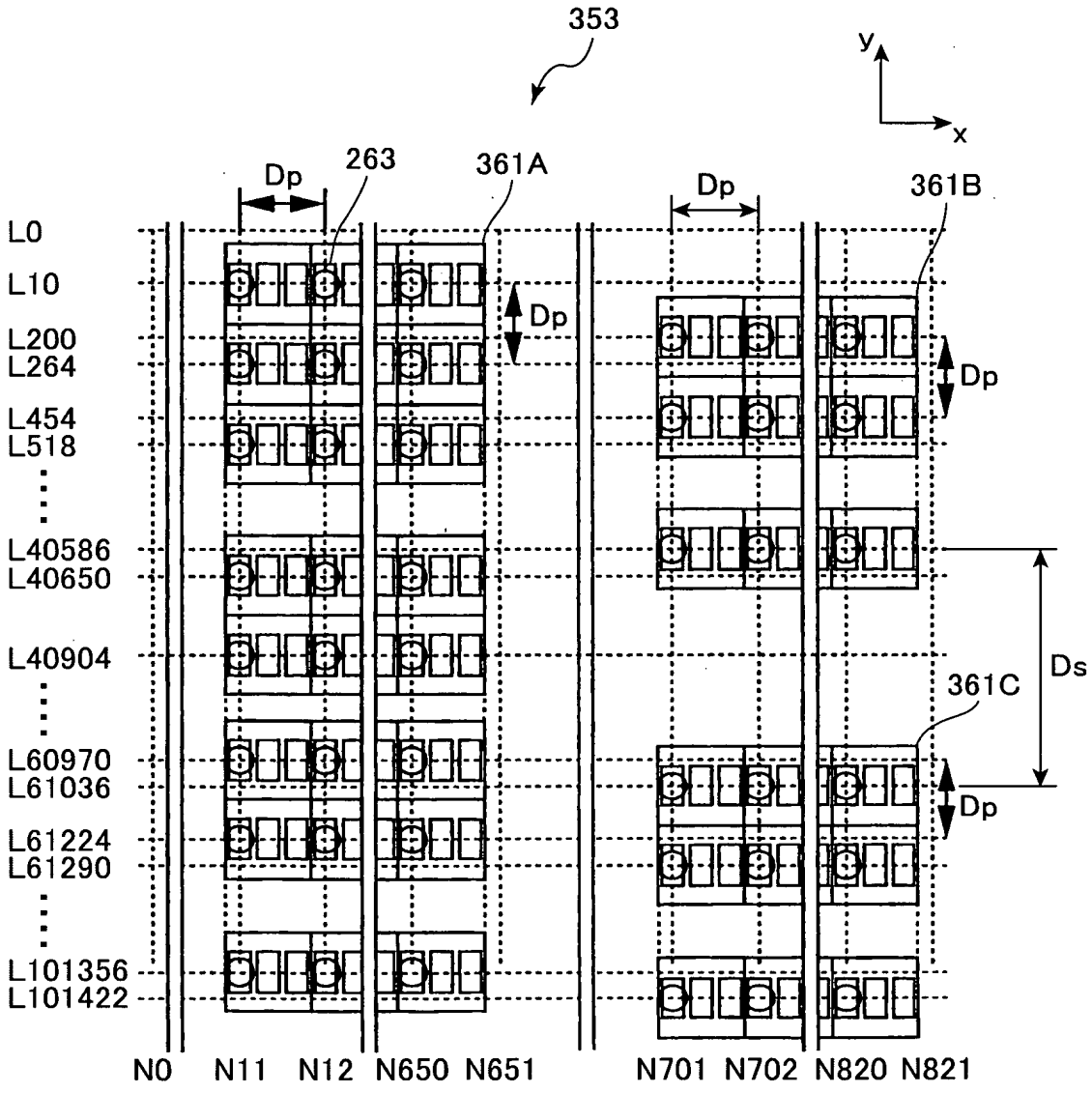

353
y
x
Dp
263
361A
Dp
361B
L0
L10
L200
L264
L454
L518
L40586
L40650
L40904
L60970
L61036
L61224
L61290
L101356
L101422
Dp
Dp
Ds
361C
Dp
N0
N11
N12
N650
N651
N701
N702
N820
N821

FIG.10

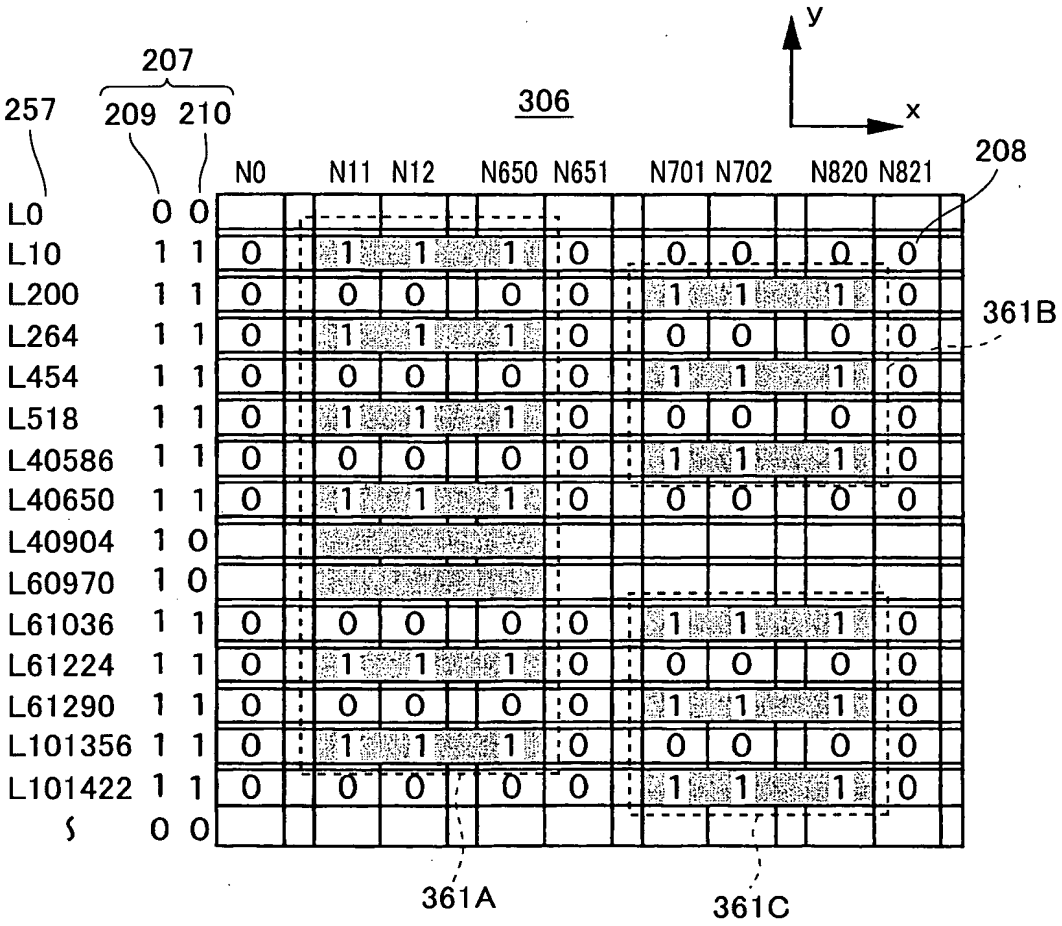

y
x
207
257
209
210
306
208
N0
N11
N12
N650
N651
N701
N702
N820
N821
L0 0 0
L10 1 1 0 1 1 1 0 0 0 0 0
L200 1 1 0 0 0 0 0 1 1 1 0
L264 1 1 0 1 1 1 0 0 0 0 0
L454 1 1 0 0 0 0 0 1 1 1 0
L518 1 1 0 1 1 1 0 0 0 0 0
L40586 1 1 0 0 0 0 0 1 1 1 0
L40650 1 1 0 1 1 1 0 0 0 0 0
L40904 1 0
L60970 1 0
L61036 1 1 0 0 0 0 0 1 1 1 0
L61224 1 1 0 1 1 1 0 0 0 0 0
L61290 1 1 0 0 0 0 0 1 1 1 0
L101356 1 1 0 1 1 1 0 0 0 0 0
L101422 1 1 0 0 0 0 0 1 1 1 0
S 0 0
361A
361B
361C

FIG.11

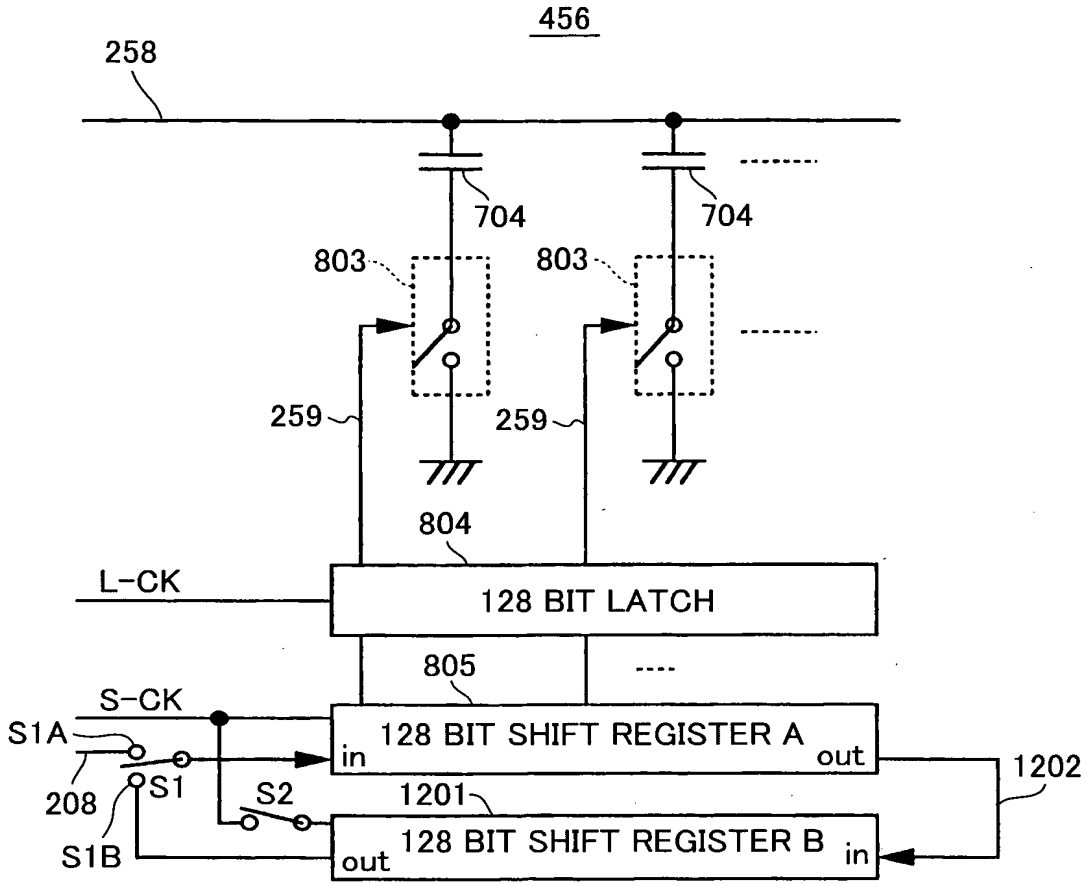


FIG.13

		M0	M1	M2	M3	M4
407 1101	DRIVE WAVEFORM GENERATION	0	1	1	1	1
407 1102	COATING DATA TRANSFER	0	0	0	1	1
407 1103	DATA ROTATION	*	0	1	0	1
	LATCH CLOCK L-CK	0	0	1	1	1
	SHIFT CLOCK S-CK	0	0	1	1	1
408 1104	SWITCH S1	*	*	S1B	S1A	S1A
408 1105	SWITCH S2	*	*	CLOSE	OPEN	CLOSE

FIG.12

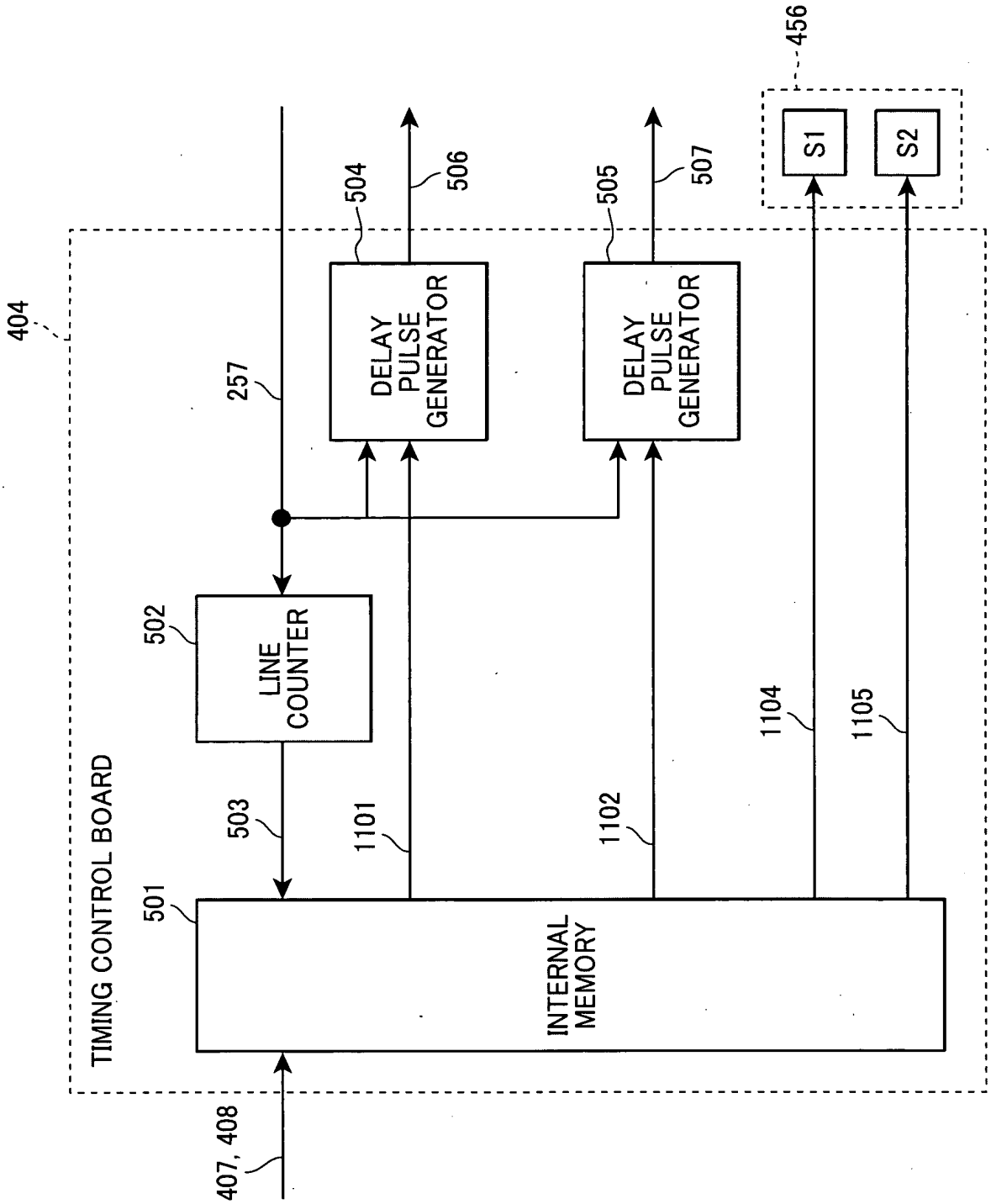
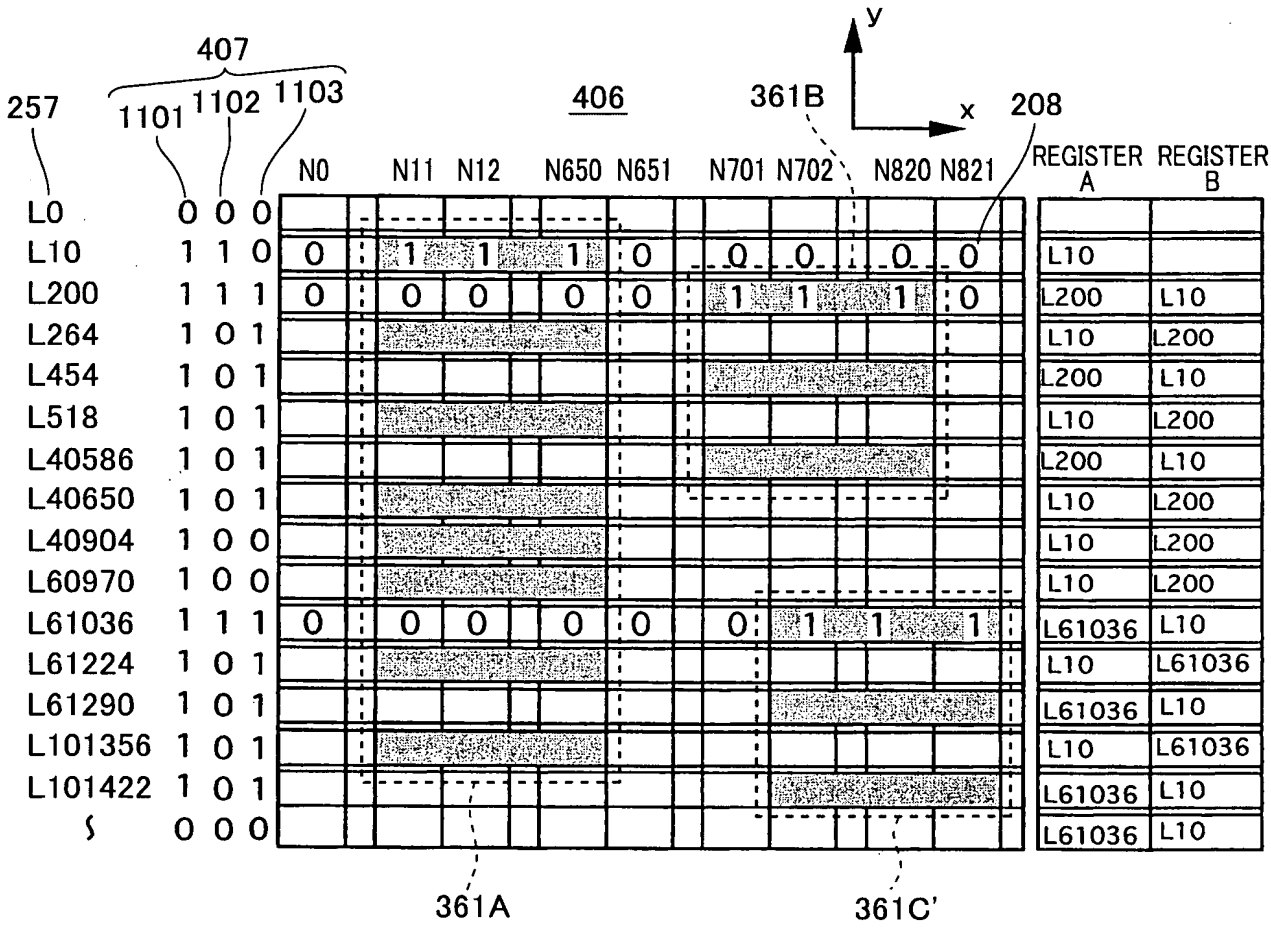

456
S1
S2
504
506
505
507
404
257
DELAY PULSE GENERATOR
DELAY PULSE GENERATOR
502
LINE COUNTER
1104
1105
503
1101
1102
501
INTERNAL MEMORY
TIMING CONTROL BOARD
407, 408

FIG.14


257
407
1101
1102
1103
406
361B
y
x
208
N0
N11
N12
N650
N651
N701
N702
N820
N821
REGISTER A
REGISTER B
L0 0 0 0
L10 1 1 0
L200 1 1 1
L264 1 0 1
L454 1 0 1
L518 1 0 1
L40586 1 0 1
L40650 1 0 1
L40904 1 0 0
L60970 1 0 0
L61036 1 1 1
L61224 1 0 1
L61290 1 0 1
L101356 1 0 1
L101422 1 0 1
S 0 0 0
L10
L200 L10
L10 L200
L200 L10
L10 L200
L200 L10
L10 L200
L10 L200
L10 L200
L61036 L10
L10 L61036
L61036 L10
L10 L61036
L61036 L10
L61036 L10
361A
361C'